Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Q12**
2. **Q6**
3. **Q5**
4. **Q7**
5. **Q4**
6. **Q3**
7. **Q2**
8. **GND**
9. **Q1**
10. **Ø**
11. **MR**
12. **Q9**
13. **Q8**
14. **Q10**
15. **Q11**
16. **VCC**

**.090”**

**.071”**

**2 1 16 15**

**7 8 9**

**14**

**13**

**12**

**11**

**10**

**3**

**4**

**5**

**6**

**MASK**

**REF**

**HC**

**4040G**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC (or FLOATING)**

**Mask Ref: HC4040G**

**Geometry: G**

**APPROVED BY: DK DIE SIZE .090” X .071” DATE: 8/30/21**

**MFG:TEXAS INSTRUMENTS THICKNESS .025” P/N: CD74HC4040**

**DG 10.1.2**

#### Rev B, 7/19/02